CLAIMS

1. An amplification circuit, comprising:

an input (V_{IN}) to which an input voltage is provided;

a capacitor arrangement (42); and

a switching arrangement,

wherein the capacitor arrangement comprises a first capacitor (C_2) which has a voltage-dependent capacitance and a second capacitor (C_1),

wherein the circuit is operable in two modes, a first mode in which the input voltage is provided to one terminal of at least the first capacitor, and a second mode in which the switching arrangement causes charge to be redistributed between the first and second capacitors such that the voltage across the first capacitor changes to reduce the capacitance of the first capacitor, the output voltage being dependent on the resulting voltage across the first capacitor.

2. A circuit as claimed in claim 1, wherein the switching arrangement comprises an input switch (S_{IN}) for selectively coupling the input voltage to the capacitor arrangement (42), and wherein in the first mode the input switch couples the input voltage to the capacitor arrangement, and in the second mode the input switch isolates the input voltage to the capacitor arrangement.

3. A switch as claimed in claim 2, wherein in the second mode a voltage (V_A, V_B) on one terminal of the first and/or second capacitor is changed.

4. A circuit as claimed in claim 3, wherein the change in voltage is on the one terminal of the first capacitor and results in a reduction in the capacitance.

5. A circuit as claimed in claim 3, wherein the second capacitor (C_1) is also voltage-dependent and wherein in the second mode a voltage on one terminal of the first and second capacitors is changed.

6. A circuit as claimed in claim 5, wherein the change in voltage on the one terminal of the second capacitor results in a reduction in the capacitance.

7. A circuit as claimed in claim 5 or 6, wherein in the second mode a voltage (V_A) on the one terminal of the first capacitor (C_2) is increased and a voltage (V_B) on the one terminal of the second capacitor (C_1) is decreased.

8. A circuit as claimed in claim 7, wherein in the second mode a voltage (V_A) on the one terminal of the first capacitor (C_2) is increased from below the input voltage to above the input voltage, and the voltage (V_B) on the one terminal of the second capacitor (C_1) is decreased from above the input voltage to below the input voltage.

9. A circuit as claimed in any one of claims 3 to 8, wherein the input switch is controlled by the voltage on the one terminal of the first capacitor.

10. A circuit as claimed in claim 9, wherein the input switch comprises a first transistor (T1) with the gate connected to the one terminal of the first capacitor.

11. A circuit as claimed in claim 10, wherein the second capacitor is also voltage-dependent, and wherein in the second mode a voltage on one terminal of the second capacitor is also changed, and wherein the input switch comprises a second transistor (T2) in parallel with the first transistor (T1), and with the gate of the second transistor connected to the one terminal of the second capacitor.

12. A circuit as claimed in claim 1, wherein the switching arrangement comprises:

a first switch or switches (S_2, S_3) coupling the input voltage to one terminal of the first and second capacitors;

second switches (S_4, S_5) coupling respective control voltages to the one terminals of the first and second capacitors; and

an input switch (S_1) coupling a reference voltage to the other terminals of the first and second capacitors.

13. A circuit as claimed in claim 12, wherein in the first mode the first switch or switches (S_2, S_3) and the input switch (S_1) are closed so that a voltage across the capacitors is dependent on the input voltage (V_{IN}), and in the second mode the second switches (S_4, S_5) are closed and the output voltage comprises the voltage on the other terminals of the first and second capacitors.

14. A circuit as claimed in claim 12 or 13, wherein the first capacitor comprises a depletion n-type MOS device.

15. A circuit as claimed in claim 14, wherein the first and second capacitors comprise depletion n-type MOS devices.

16. A circuit as claimed in claim 1, wherein the input is connected to one terminal of the first and second capacitors (C_2, C_1), and respective control voltages are coupled to the other terminals of the first and second capacitors through respective control switches (S_1, S_2) of the switching arrangement.

17. A circuit as claimed in claim 16, wherein the switching arrangement further comprises a shorting switch (S_3) connected between the other terminals of the first and second capacitors.

18. A circuit as claimed in claim 17, wherein in the first mode the control switches (S_1, S_2) are closed and the voltages across the capacitors is dependent on the input voltage (V_{IN}), and in the second mode the shorting switch (S_3) is closed and the output voltage comprises the voltage on the other terminals of the first and second capacitors.

19. A circuit as claimed in any preceding claim, wherein the or each voltage-dependent capacitor comprises a transistor with source and drain connected together, and wherein the one terminal is defined by the gate and the other terminal is defined by the connected source and drain.

20. A circuit as claimed in claim 19, wherein the transistor of the or each voltage-dependent capacitor comprises a thin film MOS transistor.

21. An active matrix device comprising an array (34) of device elements and circuitry (30,32) for generating control signals for controlling the device elements, further comprising a circuit as claimed in any preceding claim for increasing the voltage level of the control signals before supply to the device elements.

22. A device as claimed in claim 21, further comprising a latch circuit at the output of the amplification circuit.

23. An active matrix display device comprising an array of display pixels, each display element having pixel refresh circuitry comprising an amplification circuit as claimed in any one of claims 1 to 20 for amplifying the gate voltage of a control transistor (68) within the refresh circuitry.

24. A device as claimed in claim 23, wherein the refresh circuitry comprises sensing circuitry for storing a display pixel voltage on a storage capacitor arrangement (66) and writing circuitry (68) for providing a voltage to the display pixel in dependence on the stored display pixel voltage, wherein the writing circuitry comprises the control transistor (68), the gate voltage of the control transistor being provided by the storage capacitor arrangement (66), and wherein the storage capacitor arrangement comprises the capacitor arrangement of the amplification circuit.

25. An active matrix array device comprising an array of device elements, each device element in the array being provided with a circuit as claimed in any one of claims 1 to 20.

26. A device as claimed in claim 25, wherein the device elements comprise memory cells, image sensing pixels, or display pixels.

27. A method of amplifying a signal, comprising:

providing an input signal to a capacitor arrangement comprising a first capacitor (C_2) which has a voltage-dependent capacitance and a second capacitor (C_1);

causing charge to be redistributed between the first and second capacitors (C_2, C_1) such that the voltage across the first capacitor changes to reduce the capacitance of the first capacitor; and

providing an output voltage dependent on the resulting voltage across the first capacitor.